

(A)

Notice of Allowability	Application No.	Applicant(s)	
	09/687,197	MARUO, YUTAKA	
	Examiner	Art Unit	
	Khanh Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to the amendment filed on June 3, 2004.

2. The allowed claim(s) is/are 4,5,30,32-43 and 45-52.

3. The drawings filed on _____ are accepted by the Examiner.

4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some* c) None of the:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

(a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

1) hereto or 2) to Paper No./Mail Date _____.

(b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- 1. Notice of References Cited (PTO-892)
- 2. Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3. Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____
- 4. Examiner's Comment Regarding Requirement for Deposit
of Biological Material
- 5. Notice of Informal Patent Application (PTO-152)
- 6. Interview Summary (PTO-413),
Paper No./Mail Date _____.
- 7. Examiner's Amendment/Comment
- 8. Examiner's Statement of Reasons for Allowance
- 9. Other _____.

Michael Trinh
Primary Examiner

DETAILED ACTION

Response to Amendment

This Office Action is in response to the amendment filed on June 3, 2004.

Accordingly, claims 1-3, 6-29, 31 and 44 were canceled, claims 4, 34, 36 and 45-49 were amended, and new claims 50-52 were added.

Currently, claims 4, 5, 30, 32-43 and 45-52 are pending in the application.

Allowable Subject Matter

Claims 4, 5, 30, 32-43 and 45-52 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly shows or suggests all the process limitations as claimed.

Re claim 4, none of the prior art of record discloses or suggests the combined process steps of: (A) forming a pad oxide layer on a substrate; (B) forming a polishing stopper layer on the pad oxide layer, the polishing stopper layer having a predetermined pattern for a chemical-mechanical polishing, the pad oxide layer positioned between the substrate and the polishing stopper layer; (C) removing a part of the pad oxide layer and the substrate using a mask layer including at least the polishing stopper layer as a mask to form a trench; (D) forming a trench oxide film on a surface of the substrate that forms the trench; (E) forming an insulating layer that fills the trench; (F) polishing the insulating layer by a chemical-mechanical polishing; (G) removing the polishing stopper layer; (H) etching a part of the insulating layer to form a trench insulating layer and etching the pad oxide layer remaining on the substrate adjacent to the trench; and (I) after the etching the remaining pad oxide layer, forming a sacrificial oxide layer on the substrate adjacent to the trench; wherein the method further includes the step (a) of forming an

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etching stopper layer for the trench oxide film over at least a portion of the trench oxide film, wherein the etching stopper layer is a silicon nitride layer and wherein, in the step (H), the etching stopper layer is more resistant to the etching than the insulating layer wherein the etching stopper layer is formed to have an upper surface that is positioned no higher than an upper surface of the sacrificial oxide layer: and after the sacrificial oxide is formed, implanting an impurity into the substrate, and then removing the sacrificial oxide layer, wherein after the sacrificial oxide is removed, the insulating layer has an upper surface that is positioned higher than an upper surface of the etching stopper layer.

Re claim 32, none of the prior art of record discloses or suggests the combined process steps of: forming a trench comprising a lower surface and side surfaces in a silicon substrate; forming a trench oxide layer covering the lower surface and side surfaces; forming rounded corner regions at an intersection of an upper surface of the substrate and the side surfaces of the trench; forming an etch stop layer in direct contact with the trench oxide layer on the lower surface and side surfaces; filling the trench with an insulating layer directly contacting the etch stop layer, wherein the insulating layer overfills the trench and a portion of the insulation layer extends over the upper surface of the substrate; etching the insulating layer using an etchant that selectively etches the etch stop layer at a rate that is slower than that of the insulating layer, wherein the etching the insulating layer is carried out so that a first portion of the insulating layer that extends over the upper surface of the substrate is removed and a second portion of the insulating layer over the trench extends to a level above that of the upper surface of the substrate; and after the etching the insulating layer, implanting an impurity into a first region of the silicon substrate, implanting an impurity into a second region of the silicon substrate, and after the

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implanting the impurity into the second region, etching the second portion of the insulating layer, wherein the etching is controlled so that the second portion of the insulating layer extends to a level above that of the upper surface of the substrate.

Re claim 34, none of the prior art of record discloses or suggests the combined process steps of: forming a pad insulating layer on a silicon substrate; forming a polishing stopper layer on the pad insulating layer; forming a first resist layer having a specified pattern on the polishing stopper layer; etching the polishing stopper layer and the pad insulating layer using the first resist layer as a mask to yield a remaining polishing stopper layer and remaining pad insulation layer; removing the first resist layer; etching the silicon substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a trench in the silicon substrate; oxidizing surfaces in the trench; forming a silicon nitride layer on the oxidized surfaces in the trench; forming an insulating layer on the silicon nitride layer and overfilling the trench; planarizing the insulating layer that overfills the trench until the polishing stopper layer is reached; removing the remaining polishing stopper layer; etching the remaining pad insulation layer and the insulating layer so that a portion of the insulating layer extends to a level higher than that of the silicon substrate; performing at least one ion implantation while the insulation layer extends to a level higher than that of the silicon substrate; and etching the insulation layer after the at least one ion implantation so that the insulation layer extends to a level higher than that of the silicon substrate.

Re claim 36, none of the prior art of record discloses or suggests the combined process steps of: forming a pad insulating layer on a silicon substrate; forming a polishing stopper layer on the pad layer above an upper surface of the silicon substrate; forming a first resist layer

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having a specified pattern on the polishing stopper layer; etching the polishing stopper layer and the pad insulating layer using the first resist layer as a mask to yield a remaining polishing stopper layer and remaining pad insulation layer; removing the first resist layer; etching the silicon substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a trench in the silicon substrate; oxidizing surfaces in the trench; forming an etch stop layer on the oxidized surfaces in the trench and on side surfaces and an upper surface of the polishing stopper layer; forming an insulating layer on the etch stop layer and overfilling the trench; planarizing the insulating layer that overfills the trench; after the planarizing, etching the polishing stopper layer and the etch stop layer so that the polishing stopper layer is removed and the etch stop layer that extends to a level above the upper surface of the silicon substrate is removed; after the etching the polishing stopper layer, etching the remaining pad insulation layer and the insulating layer so that a portion of the insulating layer remains at a level higher than that of the silicon substrate and the etch stop layer; forming a sacrificial oxide layer on the silicon substrate; performing at least one ion implantation into the silicon substrate while the insulation layer extends to a level higher than that of the silicon substrate and the etch stop layers; and etching the sacrificial oxide layer and the insulation layer after the at least one ion implantation, wherein the etching is controlled so that the insulation layer extends to a level higher than that of the silicon substrate.

Re claim 44, none of the prior art of record discloses or suggests the combined process steps of: forming a pad insulating layer on a silicon substrate; forming a polishing stopper layer on the pad layer above an upper surface of the silicon substrate; etching the polishing stopper layer and the pad insulating layer using a mask to yield a remaining polishing stopper layer and

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remaining pad insulation layer; etching the silicon substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask. to form a trench in the silicon substrate; oxidizing surfaces in the trench; forming an etch stop layer on the oxidized surfaces in the trench and on side surfaces and an upper surface of the polishing stopper layer; forming an insulating layer on the etch stop layer and overfilling the trench; planarizing the insulating layer that overfills the trench to a level that exposes the polishing stopper layer; after the planarizing, etching the polishing stopper layer and the etch stop layer so that the polishing stopper layer is removed and the etch stop layer on the side surfaces of the polishing stopper layer is removed; and after the etching the polishing stopper layer and the etch stop layer, etching the remaining pad insulation layer and the insulating layer so that a portion of the insulating layer remains at a level higher than that of the silicon substrate and the etch stop layer; wherein the etch stop layer is formed from a non-monocrystal silicon layer selected from the group consisting of a polycrystal silicon layer, an amorphous silicon layer or a multiple layer having a polycrystal silicon layer and an amorphous silicon layer.

Re claim 47, none of the prior art of record discloses or suggests the combined process steps of: forming a pad insulating layer on a substrate; forming a polishing stopper layer on the pad insulating layer, wherein the pad insulating layer is between the substrate and the polishing stopper layer; etching the polishing stopper layer and the pad insulating layer using a mask to yield a remaining polishing stopper layer and remaining pad insulation layer; etching the substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a plurality of trenches in the substrate that are spaced apart from each other; oxidizing surfaces in the trenches; forming an etch stop layer on the oxidized surfaces in the

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trenches and on side surfaces and an upper surface of the remaining polishing stopper layer; forming an insulating layer on the etch stop layer and overfilling the trenches; planarizing the insulating layer that overfills the trenches to a level that exposes the remaining polishing stopper layer; after the planarizing, etching the remaining polishing stopper layer and the etch stop layer so that the remaining polishing stopper layer is removed and the etch stop layer on the side surfaces of the remaining polishing stopper layer is removed; after the etching the polishing stopper layer and the etch stop layer, etching the remaining pad insulation layer and a portion of the insulating layer so that the remaining pad insulation layer is removed and the substrate is exposed between the trenches; and after the etching the remaining pad insulation layer, forming an oxide layer on the exposed substrate between the trenches; performing at least one ion implantation into the substrate through the oxide layer; and etching the oxide layer and the insulation layer after the at least one ion implantation, wherein the etching is controlled so that the insulation layer extends to a level higher than that of the substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday - Thursday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



KBD



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Primary Examiner
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